UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/061,671	02/01/2002	Michael A. Filippo	5500-68500	9586

7590 12/27/2004	EXAMINER
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P.O. Box 398	ART UNIT PAPER NUMBER
Austin, TX 78767	2115

DATE MAILED: 12/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)
Office Action Summary	10/061,671	FILIPPO, MICHAEL A.
	Examiner	Art Unit
	Albert Wang	2115

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☐ Responsive to communication(s) filed on _____.
2a) ☐ This action is **FINAL**.   2b) ☒ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
   closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-16* is/are pending in the application.
   4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5) ☐ Claim(s) _____ is/are allowed.
6) ☒ Claim(s) *1-16* is/are rejected.
7) ☐ Claim(s) _____ is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.
10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
    a) ☐ All   b) ☐ Some * c) ☐ None of:
    1. ☐ Certified copies of the priority documents have been received.
    2. ☐ Certified copies of the priority documents have been received in Application No. _____.
    3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage
       application from the International Bureau (PCT Rule 17.2(a)).
    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
   Paper No(s)/Mail Date *12/03, 2/04, 8/04*.
4) ☐ Interview Summary (PTO-413)
   Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1.   Original claims 1-16 are presented for examination.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2.   Claims 1-16 are provisionally rejected under the judicially created doctrine of

obviousness-type double patenting as being unpatentable over claims 1-16 of copending

Application No. 10/061,792. Although the conflicting claims are not identical, they are not

patentably distinct from each other because the claims of copending Application are worded

nearly identically with those of the instant Application, with the exception that the copending

Application uses power control, whereas the instant Application uses clock control. Clock

control is an obvious means of power control.

This is a provisional obviousness-type double patenting rejection because the conflicting

claims have not in fact been patented.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3.   Claims 1-5, 8 and 16 are rejected under 35 U.S.C. 102(e) as being anticipated by Gabzdyl et al., U.S. Patent No. 6,202,163 ("Gabzdyl").

As per claim 1, Gabzdyl discloses an integrated device (col. 1, line 26, chip; fig. 3, digital processing circuit 201), comprising:

a plurality of functional units, wherein each functional unit is configured to receive one or more input signals, perform an operation or task, and produce one or more output signals (fig. 4, functional units (not shown) to receive control signals from decoders for instruction type 403-406; fig. 6; col. 4, lines 51-58), wherein each functional unit configured to be inactive while one or more of the other functional units is active (col. 4, lines 9-19 & 40-46);

a plurality of activity detector and clock control units coupled to said plurality of functional units (fig. 4, decoders for instruction type 403-406), wherein each activity detector and clock control unit is associated with a different one of the functional units and configured to detect when its associated functional unit will be inactive (col. 4, lines 9-19 & 40-46).

wherein each activity detector and clock control unit is configured to switch off a clock signal to its associated functional unit when its associated functional unit is inactive and provide a clock signal to its associated functional unit when its associated functional unit is active (col. 4, lines 9-19 & 40-46).

As per claim 2, Gabzdyl discloses a first one of the activity detector and clock control units is configured to monitor some or all of the input signals received by a first one of the functional units to determine if the first functional unit is inactive (fig. 5; col. 4, lines 34-46).

As per claims 3, Gabzdyl discloses the input signals received by the first functional unit comprise control signals for controlling the operation of the first functional unit, and wherein the first activity detector and clock control unit is configured to monitor one or more of the control signals to determine when the first functional unit is inactive (fig. 5; col. 4, lines 34-46).

As per claim 4, Gabzdyl discloses the input signals received by the first functional unit comprise data operated on by the first functional unit, and wherein the first activity detector and clock control unit is configured to monitor the flow of data to the first functional unit to determine when the first functional unit is inactive (fig. 5; col. 4, lines 34-46).

As per claim 5, Gabzdyl discloses the input signals received by the first functional unit comprise instructions to be performed by the first functional unit, and wherein the first activity detector and clock control unit is configured to monitor the instruction flow to the first functional unit to determine when the first functional unit is inactive (fig. 5; col. 4, lines 34-46).

As per claim 8, Gabzdyl discloses each of the activity detector and clock control units comprises:

an activity detector configured to determine when the associated functional unit is inactive (fig. 5, mux 501); and

a clock gate coupled to the activity detector and configured to receive a main clock source for the integrated device and provide a functional unit clock supply to the associated functional unit (fig. 5, clock switch 503);

wherein the activity detector is configured to control the clock gate to shut off the

functional unit clock supply for the associated functional unit when the associated functional unit

is inactive (col. 4, lines 34-46).

As per claim 16, Gabzdyl discloses an integrated device (col. 1, line 26, chip; fig. 3,

digital processing circuit 201), comprising:

a first functional unit configured to receive an first input and perform a first operation or

task according to the first input (fig. 4, functional unit (not shown) to receive control signals

from decoder for instruction type 403);

a second functional unit configured to receive a second input and perform a second

operation or task according to the second input (fig. 4, functional unit (not shown) to receive

control signals from decoder for instruction type 404);

an activity detector coupled to the first and second inputs and configured to determine

when the first function unit will be inactive and when the second functional unit will be inactive

(figs. 3 & 4, instruction decode and clock generator unit 310; col. 4, lines 9-19 & 40-46);

a first clock control unit configured to control a first clock to the first functional unit (fig.

5, clock switch 503 for decoder for instruction type 403), wherein said first clock control unit is

configured to shut off the first clock to the first functional unit when the activity detector

determines that the first functional unit will be inactive (col. 4, lines 34-46); and

a second clock control unit configured to control a second clock to the second functional

unit (fig. 5, corresponding clock switch for decoder for instruction type 404), wherein said

second clock control unit is configured to shut off the second clock to the second functional unit

when the activity detector determines that the second functional unit will be inactive (col. 5, lines

9-21).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in
> section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are
> such that the subject matter as a whole would have been obvious at the time the invention was made to a person
> having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the
> manner in which the invention was made.

4.   Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gabzdyl et al.,

U.S. Patent No. 6,202,163 ("Gabzdyl"), in view of Suzuki, U.S. Patent No. 5,987,616.

As per claim 10, Gabzdyl teaches a microprocessor (col. 1, line 26, chip; fig. 3, digital

processing circuit 201), comprising:

a first functional unit configured to receive a first-instruction-type instruction stream and

execute first-instruction-type instructions from the first-instruction-type instruction stream (fig.

4, functional unit (not shown) to receive control signals from decoder for instruction type 403;

col. 4, lines 9-19 & 40-46);

a second functional unit configured to receive a second-instruction-type instruction

stream and execute second-instruction-type instructions from the second-instruction-type

instruction stream (fig. 4, functional unit (not shown) to receive control signals from decoder for

instruction type 404; col. 4, lines 9-19 & 40-46);

a first activity detector unit coupled to the first-instruction-type instruction stream and

configured to detect when the first functional unit will be inactive and switch off a clock signal

to the first-instruction-type execution unit when it is inactive (fig. 4, decoder for instruction type 403; col. 4, lines 9-19 & 40-46); and

a second activity detector unit coupled to the second-instruction-type instruction stream and configured to detect when the second-instruction-type execution unit will be inactive and switch off a clock signal to the second-instruction-type execution unit when it is inactive (fig. 4, decoder for instruction type 404; col. 4, lines 9-19 & 40-46).

However, Gabzdyl does not expressly teach the first functional unit as an integer execution unit, and a second functional unit as a floating point execution unit. Suzuki teaches a plurality of functional units (col. 4, lines 60-65), which are activated/inactivated based upon the instruction stream (col. 5, lines 9-21). Suzuki further teaches a first functional unit as an integer execution unit, and a second functional unit as a floating point execution unit (figs. 1-6, integer operation part 8, floating point operation part 8). At the time of the invention, it would have been obvious to one of ordinary skill in the art to implement Gabzdyl's functional units as Suzuki's integer and floating point execution units, as such implementation of functional units in microprocessors is common.

5.   Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gabzdyl as applied to claim 1 above, and further in view of Fung, U.S. Patent No. 6,584,571.

As per claim 6, Gabzdyl does not expressly teach determining if an associated functional unit will be inactive for a threshold amount of time. Fung teaches determining if an associated functional unit will be inactive for a predetermined period of time (col. 5, lines 46-56). Fung also teaches a power control unit to shut off a clock to a functional unit during periods of

inactivity (col. 6, lines 43-51). At the time of the invention, it would have been obvious to one

of ordinary skill in the art to apply Fung's inactivity threshold to Gabzdyl integrated device. A

motivation for doing so would have been to prevent needless oscillating between active and

inactive states (Fung, col. 11, lines 29-31).

As per claim 7, Fung teaches the threshold amount of time varies with clock speed (col.

11, lines 26-27). In other words, the threshold amount of time is related to a predetermined

number of clock cycles.

6.   Claims 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Gabzdyl/Suzuki as applied to claim 10 above, and further in view of Fung, U.S. Patent No.

6,584,571.

As per claims 11 and 12, since Gabzdyl/Fung teaches the integrated device of claims 6

and 7 and Gabzdyl/Suzuki teaches the microprocessor of claim 10, Gabzdyl/Suzuki/Fung teaches

the claimed microprocessor.

7.   Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gabzdyl as applied

to claim 1 above, and further in view of Pappert, U.S. Patent No. 6,380,760.

As per claim 9, Gabzdyl does not expressly teach an output emulator configured to drive

the output signals for a first one of the functional units to a safe state when shut off the clock to

the first functional unit. Pappert teaches an output emulator to drive output signals to a tri-stated,

or high impedance state, when shutting off the clock to a first functional unit (fig. 1, contention

detection circuit 12; col. 2, lines 50-59; col. 3, lines 14-21). At the time of the invention, it

would have been obvious to one of ordinary skill in the art to apply Pappert's output emulator to

Gabzdyl integrated device, as a way to prevent buffer contention (Pappert, col. 1, lines 25-44).

8.   Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shiell et al., U.S.

Patent No. 6,138,232 ("Shiell"), in view of Suzuki, U.S. Patent No. 5,987,616, and Gabzdyl et

al., U.S. Patent No. 6,202,163 ("Gabzdyl").

As per claim 13, Shiell teaches a microprocessor, comprising:

an instruction fetch and decode unit configured to fetch and decode microprocessor

instructions (fig. 1, comprising fetch unit 126 through decode unit 134);

an instruction scheduler configured to receive an instruction stream from the instruction

fetch and decode unit (fig. 1, scheduler 136), wherein the instruction scheduler is further

configured to buffer the instruction stream and schedule instructions from the instruction stream

for execution (col. 5, lines 12-18);

an integer execution unit configured to receive integer instructions from the instruction

scheduler and execute the integer instructions (fig. 1, ALU 142; col. 4, lines 9-15, ALU for

processing integer operations);

a floating point execution unit configured to receive floating point instructions from the

instruction scheduler and execute the floating point instructions (fig. 1, floating point unit 130;

col. 4, lines 9-15);

an activity detector coupled to the instruction scheduler and configured to monitor the

instruction stream (figs. 2 & 4, IRET detector 217; col. 6, lines 40-50).

However, Shiell does not expressly teach the activity detector to detect a lack of instructions for the integer execution unit and to determine a lack of instructions for the floating point execution unit. Suzuki teaches coupling an activity detector to any one of a plurality of units (figs. 1-4, PMUs 3-3c are coupled to different units). Suzuki's activity detector determines a lack of instructions for either the integer execution unit or the floating point execution unit (figs. 1-4, for either integer operation part 8 or floating point part 9; col. 5, lines 9-21). At the time of the invention, it would have been obvious to one of ordinary skill in the art to coupled Suzuki's activity detector to Shiell's instruction scheduler. A motivation for doing so would have been to reduce power consumption due to subthreshold current leakage (Suzuki, col. 1, lines 10-21; col. 2, lines 33-37).

Shiell/Suzuki does not expressly teach first and second clock control circuits configured to control first and second clocks to the integer and floating point execution units. Gabzdyl teaches:

a first clock control unit configured to control a first clock to the first functional unit (fig. 5, clock switch 503 for decoder for instruction type 403), wherein said first clock control unit is configured to shut off the first clock to the first functional unit when the activity detector detects a lack of first-instruction-type instructions in the instruction stream (col. 4, lines 34-46); and

a second clock control unit configured to control a second clock to the second functional unit (fig. 5, corresponding clock switch for decoder for instruction type 404), wherein said second clock control unit is configured to shut off the second clock to the second functional unit when the activity detector detects a lack of first-instruction-type instructions in the instruction stream (col. 5, lines 9-21).

At the time of the invention, it would have been obvious to apply Gabzdyl's clock control to

Shiell/Suzuki's microprocessor, in order to selectively control power consumption (Gabzdyl, col.

1, lines 24-35).

9.   Claims 14 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Shiell/Suzuki/Gabzdyl as applied to claim 13 above, and further in view of Fung, U.S. Patent No.

6,584,571.

As per claim 14, Shiell/Suzuki/Gabzdyl does not expressly teach determining if an

associated functional unit will be inactive for a threshold amount of time. Fung teaches

determining if an associated functional unit will be inactive for a predetermined period of time

(col. 5, lines 46-56). Fung also teaches a power control unit to shut off power to a functional unit

during periods of inactivity (col. 6, lines 43-51). At the time of the invention, it would have been

obvious to one of ordinary skill in the art to apply Fung's inactivity threshold to

Shiell/Suzuki/Gabzdyl's microprocessor. A motivation for doing so would have been to prevent

needless oscillating between power-on and power-off states (Fung, col. 11, lines 29-31).

As per claim 15, Suzuki teaches the activity detector is configured to monitor the

instruction stream to detect the presence of floating point instructions in the instruction stream

and control the second power control unit to restore power to the floating point execution unit

when a floating point instruction is scheduled for the floating point execution unit (col. 5, lines 9-
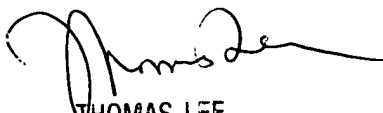
21).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Albert Wang whose telephone number is 571-272-3669. The examiner can normally be reached on M-F (9:30 - 6:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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December 10, 2004

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